IN THE CLAIMS

1. (Currently Amended) A memory system comprising:

a plurality of memory devices associated with only one processor, with each memory device comprising:

(a) an array of memory cells;

(b) an addressing circuitry operatively coupled to the array of [[the]] memory cells, wherein the addressing circuitry is capable of providing addresses to the array of memory cells;

(c) a memory device bus interface;

(d) a command decoder which decodes commands at the memory device bus interface, including an address assign command; and

(e) a local address storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once the address assign command is decoded by the command decoder; and

a memory controller having a controller bus interface coupled to the memory device bus interface, with the memory controller providing the local address to be stored in the local address storage circuitry of the memory device of the memory system together with the address assign command.

2. (Previously Presented) The memory system of claim 1, wherein the controller bus interface of the memory controller is coupled to the memory device bus interface of the memory device by a system bus.

3. (Original) The memory system of claim 2, including a plurality of the memory devices wherein the memory controller transfers the local address to the memory devices over the system bus and the address assign command over the system bus.

4-63. (Canceled)

64. (Currently Amended) A memory system comprising:

a processor;

a memory controller;

a plurality of flash memory devices associated with only one processor, with each memory device comprising:

(a) an array of memory cells;

(b) an addressing circuitry operatively coupled to the array of [[the]] memory cells, wherein the addressing circuitry is capable of providing addresses to the array of memory cells;

(c) a memory device bus interface;

(d) a command decoder which decodes commands at the memory device bus interface, including an address assign command;

(e) local address storage circuitry on each of the plurality of memory devices, wherein the local address storage circuitry is used to store a local address assigned from the memory controller that identifies a single associated memory device.

65. (Previously Presented) The memory system of claim 64, wherein the memory controller is configured to assign local addresses to each of the plurality of memory devices in a serial order.

66. (Previously Presented) The memory system of claim 64, wherein the memory controller includes an ASIC controller.

67. (Canceled)

68. (Currently Amended) A memory system comprising:

a processor;

an ASIC memory controller;

a plurality of memory devices associated with only one processor, with each memory device comprising:

(a) an array of memory cells;

(b) an addressing circuitry operatively coupled to the array of [[the]] memory cells, wherein the addressing circuitry is capable of providing addresses to the array of memory cells;

(c) a memory device bus interface;

(d) a command decoder which decodes commands at the memory device bus interface, including an address assign command;

(e) local address storage circuitry on each of the plurality of memory devices, wherein the local address storage circuitry is used to store a local address assigned from the memory controller that identifies a single associated memory device; and

a system bus coupled between the memory controller and the plurality of memory devices to transfer the local address.

69. (Canceled)

70. (Currently Amended) The memory system of claim 68, wherein the [[a]] plurality of memory devices ~~include~~ includes a plurality of flash memory devices.

71. (Currently Amended) A memory system comprising:

at least one processor;

a memory controller;

a plurality of memory devices associated with only one processor, each memory device being connected to the memory system in a memory expansion socket, with each memory device comprising:

(a) an array of memory cells;

(b) an addressing circuitry operatively coupled to the array of [[the]] memory cells, wherein the addressing circuitry is capable of providing addresses to the array of memory cells;

(c) a memory device bus interface;

(d) a command decoder which decodes commands at the memory device bus

interface, including an address assign command;

(e) local address storage circuitry on each of the plurality of memory devices, wherein the local address storage circuitry is used to store a local address assigned from the memory controller that identifies a single associated memory device.

72. (Previously Presented) The memory system of claim 71, wherein the memory controller includes an ASIC controller.

73. (Currently Amended) The memory system of claim 71, wherein the [[a]] plurality of memory devices ~~include~~ includes a plurality of flash memory devices.

74. (Previously Presented) The memory system of claim 71, further including a second processor and a plurality of memory devices associated with only the second processor.